

Computer Engineering OLD IES questions

IES-1999

1. The expression for the infix equivalent of the prefix form of $+ - * \uparrow ABCD/EF + GH$ will be

- a. $B^{B^*C} - D + E/F/G+H$
- b. $A^B * C - D+E/F/G+H$
- c. $A^B * C - D+E/F/(G+H)$
- d. $A^B * C - D+E/(F/(G+H))$

2. A PASCAL function is defined as `calc (var A: real ; B: real): real; begin`

`X: = 3.0;`

`Y: 3.0;`

`R; = calc (X, Y);`

The value of R would be

- a. 15
- b. 29
- c. 13
- d. 31

3. Consider the following statements:

- 1. An assembly language program runs faster than a high level language program to produce the desired result.
- 2. An assembler which runs on a computer for which it produces object codes is called a resident assembler.
- 3. A cross-assembler is an assembler that runs on a computer than that for which it provides machine codes.
- 4. A one-pass assembler reads the assembly language programs only once.

Which of these statements are correct?

- a. 1, 2 and 3
- b. 2, 3 and 4
- c. 1 and 4
- d. 1, 2, 3 and 4

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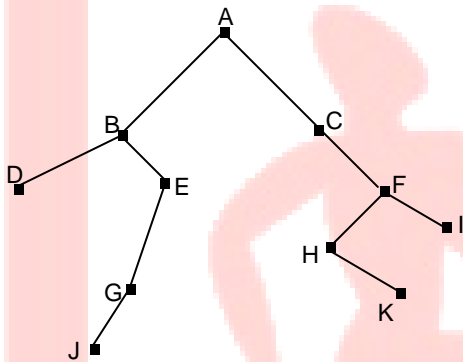
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4. The principle of locality of reference justifies the use of
- a. interrupts
 - b. DMA
 - c. virtual memory
 - d. cache memory

5. If the given binary tree is traversed in post order



Then the order of nodes visited is

- a. J G E D B K H I F C A
- b. D B J G E A K H F I C
- c. D J G E B K H I F C A
- d. A B D E G J C F H K I

6. Consider the following features:

- 1. Negative operands cannot be used.
- 2. When immediate operand changes, the program should be reassembled.
- 3. The program is difficult to read.
- 4. The size of operand is restricted by word length of the computer.

Disadvantages of immediate addressing include

- a. 1 and 2
- b. 2 and 4

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c. 2 and 3

d. 1 and 4

7. The method used to transfer data from I/O units to memory by suspending the memory CPU data transfer for one memory cycle is called

a. I/O spooling b. cycle stealing

c. line conditioning d. demand paging

8. The access time of a word in a 4 MB main memory is 100 ns. The access time of a word in a 32 kB data cache memory is 10 ns. The average data cache hit ratio is 0.95. The effective memory access time is

a. 9.5 ns

b. 14.5 ns

c. 20 ns

d. 95 ns

9. In 8086 microprocessor if the code segment register contains 1FAB and IP register contains 10A1, the effective memory address is

a. 20B51

b. 304C

c. FBC0

d. FDB5

10. To have the multiprocessing capabilities of the 8086 microprocessor, the pin connected to the ground is

a. \overline{DEN}

b. ALE

c. INTR

d. MN/\overline{MX}

11. Assertion (A): The top down structured programming should be used for developing programs.

Reason (R): The top down structured programming methodology enables us to get readable and easily provable programs.

a. Both A and R are true and R is the correct explanation of A

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- b. Both A and R are true but R is not the correct explanation of A
- c. A is true but R is false
- d. A is false but R is true

12. Assertion (A): The 'do-while' statements is used less frequently than the while statement.

Reason (R): For most applications, it is more natural to test for continuation of a loop at the beginning rather than at the end of the loop.

- a. Both A and R are true and R is the correct explanation of A
- b. Both A and R are true but R is not the correct explanation of A
- c. A is true but R is false
- d. A is false but R is true

13. Match List-I (Pre terminals) with List-II (Applications) and select the correct answer using the code given below the lists:

List-I

- a. SID, SOD
- b. Ready
- c. TRAP
- d. ALE

List-II

- 1. Wait state
- 2. Interrupt
- 3. Serial data transfer
- 4. Memory or I/O read/write
- 5. Address latch control

Codes:

- | | A | B | C | D |
|----|---|---|---|---|
| a. | 3 | 1 | 5 | 2 |
| b. | 3 | 1 | 2 | 5 |
| c. | 4 | 3 | 2 | 5 |
| d. | 4 | 3 | 1 | 2 |

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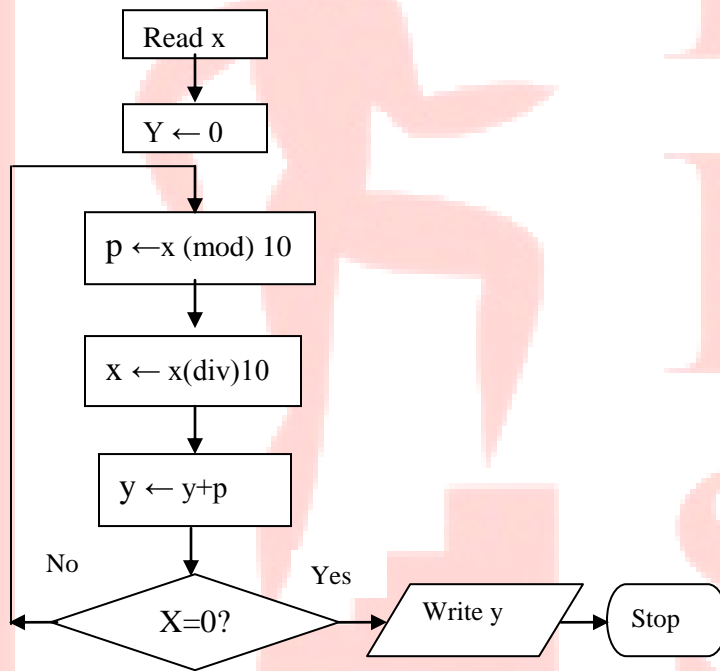
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14. The software that transfer the object program from secondary memory to the main memory is called

- a. assembler
- b. loader
- c. linker
- d. task builder

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15. If the value of x in decimal number 3954, the value of y in decimal number computed by the given flow chart is



- a. 20
- b. 22
- c. 21
- d. 3954

16. In C language, f - = 9 is equivalent to

- a. f = -9
- b. f = f-9
- c. f= 9 -1
- d. - f = 9

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17. A primitive computer uses a single register. The following fragment of assembly code is written for the machine

LOAD X

MULTY

STORE T 1

MULT 1

STORE T 1

LOAD Z

ADD Z

ADDT 1

STORE R

Which one of the following expressions is evaluated?

a. $R: = (XY) + Y + Z$

b. $R: (XY)^2 + Y + Z$

c. $R: = XY^2 + Y + Z$

d. $R: XY^2 (Y + Z)$

18. A single edge is added to a tree without increasing the number of nodes. The number of cycles in the resulting graph is equal to

a. zero

b. one

c. two

d. indeterminate

19. The prefix form of the expression $X + Y - Z$ is

a. $- +XYZ$

b. $+ - XYZ$

c. $XYZ - +$

d. $XYZ + -$

20. Consider the following statements:

The horizontal microinstruction has

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1. longer control word than vertical microinstruction.
2. high degree of parallelism
3. slower execution than vertical micro instruction

Which of these statements is/are correct?

- a. 1 alone b. 2 alone
c. 1 and 2 d. 2 and 3

21. The logic operation that will selectively clear bits in register A in those positions where there are 1's in the bits of register B is given by

- a. $A \leftarrow A + B$ b. $A \leftarrow \bar{A}B$
c. $A \leftarrow \bar{A} + \bar{B}$ d. $A \leftarrow A\bar{B}$

22. Which one of the following is loaded in the main memory by the bootstrap loader?

- a. System data b. User program
c. BIOS d. Parts of DOS

23. If a Ram has 34 bits in its MAR and 16 bits in its MDR, then its capacity will be

- a. 32 GB b. 16 GB
c. 32 MB d. 16 MB

24. In 8086, if the content of the code segment register is 1FAB and the content of the IP register is 10 A 1, then the effective memory address is

- a. 1FBC0 b. 304C
c. FDB5 d. 20B51

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25. Assertion (A): Most personal computers use static RAMs for their main memory.

Reason (R): Static RAMs are much faster than dynamic RAMs.

- a. Both A and R are true and R is the correct explanation of A
- b. Both A and R are true but R is not the correct explanation of A
- c. A is true but R is false
- d. A is false but R is true

26. Assertion (A): LRU (Least Recently used) replacement policy is not applicable to direct mapped caches.

Reason (R): A unique memory page is associated with every cache page in direct mapped caches.

- a. Both A and R are true and R is the correct explanation of A
- b. Both A and R are true but R is not the correct explanation of A
- c. A is true but R is false
- d. A is false but R is true

27. Consider the following instructions executed in 8086.

PUSH AX; AX has 20 Hex in it

PUSH BX; BX has 34 Hex in it

POP AX;

ADD AX, BX;

POP G

The value stored in G would be

- a. 20 Hex
- b. 34 Hex
- c. 54 Hex
- d. 68 Hex

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28. Which of the following conditional if statements of Pascal are correct?

1. If condition 1 THEN statement 1

ELSE IF condition 2 THEN statement 2 ELSE statement 3

2. If condition 1 THEN IF condition 2 THEN statement 1 ELSE statement 2 ELSE statement 3

3. IF condition 1 THEN IF condition 2 THEN statement 1 ELSE statement 2

Select the correct answer using the codes given below:

a. 1 and 2

b. 2 and 3

c. 1 and 3

d. 1, 2 and 3

29. In an assembler which one of the following is required for variable names in symbol table.?

a. Addresses

b. Values

c. Registers

d. Storage

30. Which of the following operations are performed on linear queues?

1. Testing a linear queue for underflow

2. Enqueue operation

3. Dequeue operation

4. Testing a linear queue for overflow

Select the correct answer using the codes given below:

a. 1, 2 and 3

b. 2, 3 and 4

c. 1, 3 and 4

d. 1, 2, 3, and 4

31. Effective address is calculated by adding or subtracting displacement value to

a. immediate address

b. relative address

c. absolute address

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d. base address

32. The micro programs provided by a manufacturer to be used on his micro programmed computer are generally called

- a. software
- b. netware
- c. firmware
- d. hardware

33. The control logic for a binary multiplier is specified by a state diagram. The state diagram has four states and two inputs. To implement it by the sequence register and decoder method

- a. two flip-flops and 2 x 4 decoders are needed
- b. four flip-flops and 2 x 4 decoders are needed
- c. four flip-flops and 3 x 9 decoders are needed

34. The frequency of the driving network connected between pins 1 and 2 of a 8085 chip must be

- a. equal to the desired clock frequency
- b. twice the desired clock frequency
- c. four times the desired clock frequency
- d. eight times the desired clock frequency

35. The 8086 arithmetic instructions work on

- 1. signed and unsigned numbers
- 2. ASC II data
- 3. unpacked BCD data

Select the correct answer using the codes given below:

- a. 1 and 2
- b. 2 and 3
- c. 1 and 3
- d. 1, 2 and 3

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36. Which of the following are required for a multimedia PC?

1. CD-ROM drive, speaker and sound card.
2. Modem and network card.
3. Hardware needed to display videos and animation
4. Software needed to display videos and animation

Selection the correct answer using the codes given below:

- a. 1, 2 and 3 b. 1, 2, 3 and 4
c. 1, 2 and 4 d. 1, 3 and 4

37. Assertion (A): A processor can reference a memory stack without specifying an address.

Reason (R): The address is always available and automatically updated in the stack pointer.

- a. Both A and R are true and R is the correct explanation of A
b. Both A and R are true but R is not the correct explanation of A
c. A is true but R is false
d. A is false but R is true

38. Assertion (A): Some redundancy is useful in programming language syntax.

Reason (R): Redundancy makes a program easier to read and also allows more error-checking to be done during translation. a. Both A and R are true and R is the correct explanation of A

- b. Both A and R are true but R is not the correct explanation of A
c. A is true but R is false
d. A is false but R is true

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39. Consider the following:

1. Sign Flag
2. Zero Flag
3. Carry Flag
3. Parity Flag

Which of the above flags of 8085 get affected by the instruction SUB B?

- a. 1 and 2
- b. 1 and 3
- c. 3 and 4
- d. 1, 2, 3 and 4

40. The use of a cache in a computer system increases the

- a. available memory space for the program
- b. available memory space for data
- c. average speed of memory access
- d. addressing range of CPU

41. Consider the following:

1. Input device
2. Arithmetic and logic unit
3. Control unit
4. Auxiliary memory
5. Main memory
6. Active hub

Which of these form part of CPU?

- a. 1, 4 and 6
- b. 2, 3 and 6
- c. 2, 4 and 5
- d. 2, 3 and 5

42. Which one of the following is not a characteristic of RISC processor design?

- a. One instruction per cycle
- b. Register-to-register operations only
- c. Simple address modes

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d. Register-to-memory operations only

43. The following micro operations are part of interrupt cycle of a control unit:

1. $MAR \leftarrow \text{save address}$

$PC \leftarrow \text{routine address}$

2. $MBR \leftarrow (PC)$

3. $\text{Memory} \leftarrow (MBR)$

Which of the following is the correct order of their occurrence?

a. 1, 2 and 3 b. 2, 3 and 1

c. 2, 1 and 3 d. 3, 1 and 2

44. Which of the following is not a characteristic of transparent DMA mode of I/O operation?

a. The external logic steals cycles from the CPU

b. The normal rate of execution is slowed down

c. Only one word can be transferred at a time

d. Data is transferred to/from memory directly

45. The contents of accumulator in a 8085 microprocessor are altered after the execution of the instruction?

a. $CMP\ C$ b. $CPI\ 3A$

c. $ANI\ SC$ d. $ORA\ A$

46. An 8085 microprocessor after the execution of $XRA\ A$ instruction

a. the carry flag is set

b. the accumulator contains FF_H

c. the content of accumulator is shifted by one

d. the zero flag is set

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47. A microprocessor has 24 address lines and 32 data lines. If it uses 10 bits of opcode, the size of its Memory Buffer Register is

- a. 22 bits
- b. 24 bits
- c. 32 bits
- d. 14 bits

48. In the 8086 instruction ADD DX, [BX] [CI], the addressing mode of source operand is

- a. Register
- b. Register Indirect
- c. Based Indexed
- d. Direct

49. The Modem is used with a personal computer to do which of the following?

- a. Convert from serial to parallel and vice versa
- b. Convert signals between TTL and RS 232 C standard and vice versa
- c. Convert from digital to analog signals and vice versa
- d. To convert the computer to a long distance communication link

50. The technology used for display in PC note-books (laptop computers) is

- a. Light Emitting Diodes display
- b. Liquid Crystal display
- c. CRT display
- d. Plasma display

51. The computer program which converts statements written in high level language to object code is known as

- a. Assembler
- b. Compiler
- c. Disassembler
- d. Operating system

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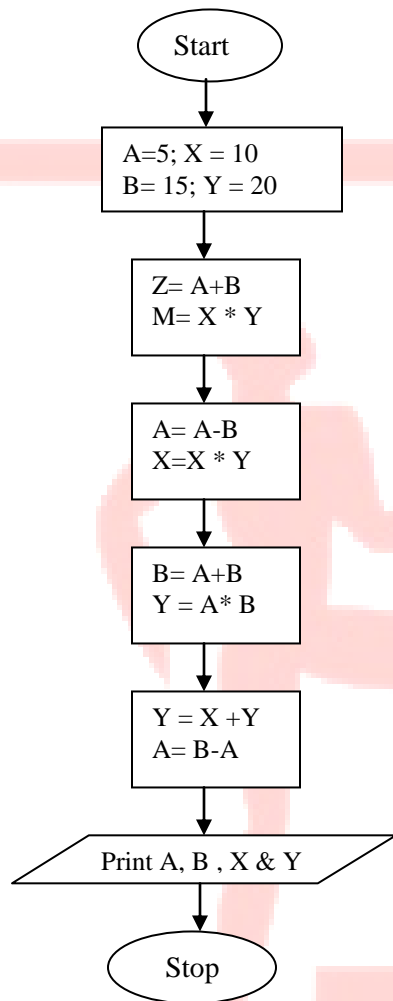
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52. What will be values of A and B, respectively, when printed for the given flow chart?



- a. 10 and 20 b. 5 and 15
c. 20 and 10 d. 15 and 5

53. Consider the following C structure and declaration:

```
structure date {  
int day ;
```

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int month ;

int year;

};

Struct data * pd:

Which of the following is the correct method to refer to the year number?

- a. (*pd). Year b. (* pd)* year
c. (* pd) → year d. pd → year

54. The different classes of formal parameters used in PASCAL are

- a. value and variable parameters
b. procedure and function parameters
c. value, variable, procedure and function parameters
d. variable, procedure and function parameters

55. Which one of the following is not a linear data structure?

- a. Array b. Linked list
c. Stack d. Tree

56. A data structure in which insertions and deletions are possible at either end, is called a

- a. queue b. deque
c. stack d. enqueue

57. Consider the following registers:

1. Accumulator and B register
2. B and C registers
3. D and E registers
4. H and L registers

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Which of these 8-bit registers of 8085 μ p can be paired together to make a 16-bit register?

- a. 1, 3 and 4 b. 2, 3 and 4
c. 1 and 2 d. 1, 2 and 3

58. Consider the following instructions of 8085 μ p.

1. MOV M, A 2. ADD C
3. MVI A, FF 3. CMP M

Which of these cause changes in the status of flag(s)?

- a. 1 and 2 b. 1, 2 and 3
c. 3 and 4 d. 2 and 4

59. A Read/Write memory chip has a capacity of 64 kBytes. Assuming separate data and address lines and availability of chip enable signal. What is the minimum number of pins required in the IC chip?

- a. 28 b. 26
c. 24 d. 22

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60. Consider the following features in an 8085 microprocessor system with memory mapped I/O.

1. I/O devices have 16-bit addresses.
2. I/O devices accessed using IN and OUT instructions
3. There can be maximum of 256 input devices and 256 output devices.
4. Arithmetic and logic operations can be directly performed with the I/O data

Select the correct answer using the codes given below:

- a. 1, 2 and 4 b. 1, 3 and 4
c. 2 and 3 d. 1 and 4

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61. In 8085 microprocessor the value of the most significant bit of the result following the execution of any arithmetic or Boolean instruction is stored in

- a. The carry-status flag
- b. The auxiliary carry status flag
- c. The sign status flag
- d. The zero status flag

62. In a microprocessor when a CPU is interrupted it

- a. Stops execution of instructions
- b. Acknowledges interrupt and branches of subroutine
- c. Acknowledges interrupt and continues
- d. Acknowledges interrupt and waits for the next instruction from the interrupting device.

63. A certain well-known computer family represents the exponents of its floating point numbers as 'Excess- 64' integers. Which one of the following numbers is represented by the exponent $e_6 e_5 e_4 e_3 e_2 e_1 e_0$?

a.
$$e = -64 + \sum_{i=0}^6 2^i e_i$$

b.
$$e = -64 + \sum_{i=0}^6 2e_i$$

c.
$$e = 64 - \sum_{i=0}^6 2^i e_i$$

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d.
$$e = 64 - \sum_{i=0}^6 2e_i$$

64. Which one of the following correctly defines a C-macro for computing the square?

- a. # defines sqr (x) x * x
- b. # defines sqr (x) (x * x)
- c. # defines sqr (x) ((x) * (x))
- d. # defines sqr (x) (x) * (x)

65. Consider the following declaration of C : in (* P) ();

Which of the following is true for the above declaration?

- a. P is pointed to function returning integer
- b. P is pointer to an array of integers
- c. P is an array of pointers
- d. P is a function returning pointer to integer

66. Consider the following Pascal program fragment:

Var I, integer;

Procedure Y (p, q ; integer);

Begin

p:p-q;

q:p+q;

p:q-p

end;

i: = 2,

j : = 3;

Y(i, j);

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If both parameters to Y are passed by reference what are the values of i and j at the end of the program fragment?

- a. i = 0, j = 2 b. i = 1, j = 5
c. i = 2, j = 3 d. i = 3, j = 2

67. Consider the following C program:

```
#include <stdio.h >
main ( )
{ float total = 0.0, q = 1.0, p = 2.0, while (p/ q> 0.001)
  {
    q = q+q;
    total = total + P/q;
    print f ("% f\n". total);
  }
}
```

Which one of the following is the integer that best approximate the last number printed?

- a. 0 b. 1
c. 2 d. 3

68. Which of the following correctly declares a pointer to an array of integers in C?

- a. int * P[20]; b. int * P ;
c. int (* P)[20]; d. int * (P [20]);

69. Consider the assembler directives:

ORG 8000
T: DW OFAOFH

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Which one of the following is correct?

- a. The contents of the locations 8000 and 8001 get erased
- b. The contents of the locations 8000 and 8001 remain unchanged
- c. The least significant byte OF will be stored at location 8000 and the most significant byte FA will be stored at location 8001
- d. The least significant byte OF will be stored at location 8001 and the most significant byte FA will be stored at location 8000

70. Consider the following information:

An array $A [1 \dots m]$ is said to be p -ordered if $A(i-p) \leq A[i] \leq A [i+p]$

For each i such that $p < i \leq m - p$. For example, the array 1 4 2 6 3 7 5 8 is 2-ordered.

In a 2-ordered array of $2N$ elements, what is the maximum number of positions that an element can be from its position if the array were 1-ordered?

- a. 1
- b. 2
- c. $N/2$
- d. N

71. Which of the following are included in the architecture of computer?

- 1. Addressing modes, design of CPU
- 2. Instruction set. Data formats
- 3. Secondary memory, operating system.

Select the correct answer using the codes given below:

- a. 1 and 2
- b. 2 and 3
- c. 1 and 3
- d. 1, 2 and 3

72. The content of which of the following determines the state of the CPU at the end of the execute cycle (when the interrupt is recognized)?

- 1. Program counter

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2. Processor register

3. Certain status conditions

Select the correct answer using the codes given below

a. 1 and 2

b. 2 and 3

c. 1 and 3

d. 1, 2 and 3

73. The first machine cycle of an instruction is always

a. A memory read cycle

b. A fetch cycle

c. An I/O read cycle

d. A memory write cycle

74. Match List-I (Type of Memory) with List-II (used as) and select the correct answer using the code given below the lists:

List-I

a. DRAM

b. SRAM

c. Parallel Access

d. ROM

List-II

1. Cache memory

2. Main memory

3. BIOS memory

4. CPU registers

Codes:

	A	B	C	D
a.	1	2	3	4
b.	2	1	4	3
c.	1	2	4	3
d.	2	1	3	4

75. PUSH a

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PUSH b
PUSH c
POP AX
POP BX
SUB AX, BX
POP BX
ADD AX, BX

The expression computed by the above program and stored in AX is

- a. $a+b-c$ b. $c+b-a$
c. $c-b+a$ d. $c-b-a$

76. Match List-I (8085 Register) with List-II (8086 Register) and select the correct answer using the code given below the lists:

List-I	List-II
a. A	1. CJ
b. H	2. AL
c. L	3. BL
d. B	4. BH

Codes:

	A	B	C	D
a.	4	2	3	1
b.	2	4	1	3
c.	4	2	1	3
d.	2	4	3	1

77. Consider the Motorola 68008, 68010, 68012 and 68020 microprocessors. In systems that are severely constrained by the space available for the printed circuit board, it is better to use

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- a. 68008 b. 68010
c. 68012 d. 68020

78. Assertion (A): In call-by-value parameter passing technique, function call overheads are less as compared to that of call by inference.

Reason (R): In call-by-reference parameter passing technique address of actual parameter is pushed into the stack.

- a. Both A and R are true and R is the correct explanation of A
b. Both A and R are true but R is not the correct explanation of A
c. A is true but R is false
d. A is false but R is true

79. Assertion (A): Insertion and deletion in a sorted array can be time-consuming.

Reason (R): All the elements following the inserted or deleted element must be shifted approximately.

- a. Both A and R are true and R is the correct explanation of A
b. Both A and R are true but R is not the correct explanation of A
c. A is true but R is false
d. A is false but R is true

80. Assertion (A): Reduced instruction set computers (RISC) use pipelined control unit.

Reason (R): Pipelining reduces memory requirements of programs.

- a. Both A and R are true and R is the correct explanation of A
b. Both A and R are true but R is not the correct explanation of A
c. A is true but R is false
d. A is false but R is true

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81. Assertion (A): The data which is keyed in can be viewed through a visual display unit (VDU).

Reason (R): VDU is also called a terminal

- a. Both A and R are true and R is the correct explanation of A
- b. Both A and R are true but R is not the correct explanation of A
- c. A is true but R is false
- d. A is false but R is true

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82. Given three integer variables a, b, c where each one will take positive value.

Which one of the following expressions in C avoids overflow?

- a. $a+b-c$
- b. $b+a-c$
- c. $b-c+a$
- d. $c+a+b-c-c$

83. $x = 1; y = 0;$

```
while y < k do
```

```
begin
```

```
x := 2 * x;
```

```
y := y+1
```

```
end;
```

For the above Pascal program fragment involving integers x, y, and k, which one of the following is a loop invariant; i.e. true at the beginning of each execution of the loop and at the completion of the loop?

- a. $x = 2^y$
- b. $x = y+1$
- c. $x = (y+1)^2$
- d. $x = (y+1) 2^y$

84. Consider the following 'C' program:

```
main ( )
```

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```
{  
Pri (); pri (); pri ()  
}  
pri ()  
{  
Static int k;  
Print ( “% d”, ++ k);  
}
```

Which one of the following is correct in respect of the program given above?

- a. It print 012
- b. It prints 123
- c. It prints 111
- d. It print 3 consecutive but unpredictable

85. Consider a complete graph with n vertices. What is the total number of spanning trees?

- a. $\frac{n(n-1)}{2}$
- b. $2n-1$
- c. $n!$
- d. n^{n-2}

86. It given that two pointer variables p and q are of the same type and $p < q$.

Which one of the following operations is logically not correct?

- a. $p - q$
- b. $p+q$
- c. $p+5$
- d. $p ++$

87. Match List-I (Type of Data Structure) with List-II (Used in Application) and select the correct answer using the code given below the lists:

List-I

List-I

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- | | |
|-----------|--|
| a. Stack | 1. Solving linear simultaneous equations |
| b. Tree | 2. Subroutine linkage |
| c. Record | 3. File processing D. Array |
| d. Array | 4. Sorting |

Codes:

	A	B	C	D
a.	3	4	2	1
b.	2	1	3	4
c.	2	4	3	1
d.	3	1	2	4

88. What is the depth of a complete binary tree with 'n' nodes?

- | | |
|----------------------|----------------------|
| a. $\log_2(n+1) - 1$ | b. $\log_2(n-1) + 1$ |
| c. $\log_2(n) + 1$ | d. $\log_2(n) - 1$ |

89. A disc drive has a average seek time of 10ms, 32 sectors on each track and 512 bytes per sector. If the average time to read 8 k bytes of continuously stored data is 20 ms, what is the rotational speed of the disc drive?

- | | |
|-------------|-------------|
| a. 3600 rpm | b. 6000 rpm |
| c. 3000 rpm | d. 2400 rpm |

90. Given a 32-bit processor with 16 MB main memory, 32 kB 4-way set-associative on chip cache and a cache block size (or line size) of 16 words. What is the total number of tag bits in the memory address format?

- | | |
|-------|-------|
| a. 9 | b. 20 |
| c. 11 | d. 24 |

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91. Match List-I (Characteristics) with List-II (Processor Architecture) and select the correct answer using the code given below the lists:

List-I

List-II

- | | |
|--------------------------------|---------------------------------------|
| a. Micro-code for CISC | 1. Both RISC and several instructions |
| b. Lack of indirect addressing | 2. CISC only |
| c. Presence of on-chip CISC | 3. Neither RISC nor cache |
| d. Simple optimizing compiler | 4. RISC only |

Codes:

- | | A | B | C | D |
|----|---|---|---|---|
| a. | 2 | 4 | 1 | 3 |
| b. | 1 | 3 | 2 | 4 |
| c. | 2 | 3 | 1 | 4 |
| d. | 1 | 4 | 2 | 3 |

92. A disc drive has a rotational speed of 3600 rpm, an average seek time of 10 ms, 64 sectors per track and 512 bytes of data per sector. What is the average time to access the entire data of a 16 k bytes file stored sequentially on the disk?

- | | |
|-------------|----------|
| a. 18.85 ms | b. 10 ms |
| c. 27.15 ms | d. 9 ms |

93. A particular parallel program computation requires 100 seconds when executed on a single processor. If 40 percent of this computation is 'inherently sequential', then what are the theoretically best elapsed times for this program running with 2 and 4 processors, respectively?

- a. 20 and 10 seconds
- b. 30 and 15 seconds
- c. 50 and 25 seconds

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d. 70 and 55 seconds

94. Consider the following statements:

The advantage of cycle stealing in DMA is that

1. It increases the maximum I/O transfer rate.
2. It reduces the interference by the DMA controller in the CPU's memory access.
3. It is beneficially employed for I/O devices with shorter bursts of data transfer.

Which of the statements given above are correct?

- a. 1 and 2 b. 1 and 3
c. 2 and 3 d. 1, 2 and 3

95. Consider a hypothetical processor with largest instruction length being 32-bit and 16 registers $R_0 - R_{15}$. Processor supports only following instructions:

ADD	Ri, Rj
SUB	Ri, Rj
AND	Ri, Rj
NOT	Ri
MOV	Ri, Rj
LOAD	Address//Loads with register R_0
STORE	Address//Stores the content of R_0
JUMP	Address
JZ	Address

What is the maximum number of address pins on this processor?

- a. 27 b. 28
c. 29 d. 30

96. Consider the following statements. The 8085 microprocessor will not enter into bus idle machine cycle whenever

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1. INTR interrupts is recognized
2. RS 0 x 5 is recognized
3. DAD rp instruction is executed

Which of the statements given above is/are correct?

- a. 1 only b. 2 only
c. 1 and 2 d. 2 and 3

97. Consider the following program

```
ORG      7000H
BEGIN    LXI      H, 7000H
          MOVE    A, L
          ADD     H
          JM      END
          RST     O
ENDS:    PCHL
          HLT
```

Which one of the following statements is correct?

- a. The program will halt the processor
- b. The program will be repeated infinitely
- c. The program will branch to 0007 H after
- d. The program will branch to 0000 H after JM END

98. Consider the following program intended to transfer a block of 5 bytes from A 000 H to 9000 H:

```
START:   LXI    B, 9000 H
          LXI    H, A 000H
          MVI    C, 05 H
LOOP:    MOV    A, M
```

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STAX B
INX B
INX H
DCR C
JNZ LOOP
HLT

The above program will not work because

- C Register is used as counter
- DCR C instruction will not affect zero flag
- JNZ instruction is used instead of JZ
- The first two instructions in loop should have been LDAX and MOV M, A

99. Assertion (A): The DMA technique is more efficient than the interrupt-driven technique for high volume I/O data transfer.

Reason (R): The DMA technique does not make use of the interrupt mechanism.

- Both A and R are true and R is the correct explanation of A
- Both A and R are true but R is not the correct explanation of A
- A is true but R is false
- A is false but R is true

IES-2005

100. Consider the following statements:

- Infix, Prefix and postfix notations for expressing sum of A and B are $A+B$, $+AB$, and $AB+$, respectively
- AVL tree is a binary tree in which the difference in heights between the left and the right sub tree is not more than one for every node.
- Stack data structure is used to save and retrieve information in reverse order.
- Queue data structure is known as LIFO.

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Which of the statements given above are correct?

- a. 1, 2 and 3
- b. 2, 3 and 4
- c. 1, 3 and 4
- d. 1, 2 and 4

101. Consider the following statements in respect of the expression: $A + XYZ$ (& A):

1. Result of expression may depend upon order of evaluation of operands of the operator 'x'
2. Result of expression would never depend upon order of evaluation of operands of the operator 'x'
3. XYZ is not a valid name of function

Which of the statements correctly defines temporal locality?

- a. 1 only
- b. 2 only
- c. 1 and 3
- d. 1, 2 and 3

102. Which one of the following correctly defines temporal locality?

- a. Adjacent instructions for current instruction may be needed soon
- b. Current instruction being fetched may be needed again soon
- c. Instructions temporarily residing in memory
- d. None of the above

103. Consider a function g which is taking a parameter f of type pointer to function which one of the following best describes the use of pointer to function?

- a. g can make modification in the definition of f and the change is visible after return from g
- b. g can dynamically test f and modify it
- c. Functionality of g gets customized through functionality of f
- d. F can dynamically test g and modify it

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104. A disc rotates at a speed of 7200 rpm. It has 4000 cylinders, 16 surfaces and 256 sectors per track. What is the average latency time of the disk?

- a. 8.33 ms b. 4.166 ms
c. 4.166 ms d. 8.33 μ s

105. Consider the following statements:

1. Cache memory is low cost and fast memory.
2. Cache memory is fast but costly memory.
3. performance of cache during program execution is measured by hit ratio.

Which of the following statements given above are correct?

- a. 1 and 2 b. 2 and 3
c. 3 and 4 d. 1 and 4

106. Consider the following statements:

The SIM instruction outputs the contents of accumulator to define

1. interrupt mask bit
2. interrupt pending bit
3. serial input data line
4. serial output data line

Which of the statements given above are correct?

- a. 1 and 2 b. 2 and 3
c. 3 and 4 d. 1 and 4

107. Match list-I (2 Pins of 8086) with List-II (Status) and select the correct answer using the code given below the lists:

List-I

\overline{BHE}

A_0

List-II

What is ready/written

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- | | | |
|------|---|-------------------------------|
| a. 0 | 0 | 1. 1 byte from/to odd address |
| b. 0 | 1 | 2. 1 byte from/to odd address |
| c. 1 | 0 | 3. 1 16-bit word |
| d. 1 | 1 | d. NOP |

Codes:

	A	B	C	D
a.	4	2	1	3
b.	3	1	2	4
c.	4	1	2	3
d.	3	2	1	4

108. What are the number of machine cycles n , and the types of machine cycles carried out for PUSH B?

- a. $n = 2$, fetch and memory write
- b. $n = 3$, fetch and 2 memory write
- c. $n = 3$, fetch, memory write and read
- d. $n = 3$, fetch, and 2 memory read

109. The following sequence of instructions is executed by an 8085 microprocessor:

1000	LXISP,	27 FF
1003	CALL	1006
1006	POP	H

What are the contents of the stack pointer (SP) and the HL register pair after completion of execution of these instructions?

- a. SP= 27 FF, HL = 1003
- b. SP= 27 FD, HL = 1003

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- c. SP = 27 FF, HL= 1006
- d. SP= 27 FD, HL = 1000

110. Which one of the following is not associated with a Logic analyzer?

- a. Delayed state
- b. Delayed sweep
- c. Disassembler
- d. Pre-triggering

111. In a 500 x 500 matrix, 95% of the element are zeros and these elements are randomly distributed. Which is an appropriate data structure to store this efficiently?

- a. An array
- b. A tree
- c. A list
- d. A stack

112. Match list-I with List-II and select the correct answer using the code given below the lists:

List-I

- a. immediate addressing
- b. Implied addressing
- c. Register addressing
- d. Direct addressing

List-II

- 1. LDA 30 SC
- 2. MOV A, B
- 3. LXI H, 2050
- 4. RRC

Codes:

- | | A | B | C | D |
|----|---|---|---|---|
| a. | 3 | 4 | 2 | 1 |
| b. | 2 | 1 | 3 | 1 |
| c. | 3 | 1 | 2 | 4 |
| d. | 2 | 4 | 3 | 1 |

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113. Match List-I (Operator of C Language) with List-II (Characteristic of the operator) and select the correct answer using the code given below the lists:

List-I	List-II
a. ^	1. unary operator
b. &	2. Binary operator
c. mod	3. Ternary operator
d. ?	4. Invalid operator

Codes:

	A	B	C	D
a.	2	1	4	3
b.	4	3	2	1
c.	2	3	4	1
d.	4	1	2	3

114. What is the output of the following program?

```
#include < Stdio. h>
main ( )
{
float f;
f = 10/3
print f ( “ % f, “f);
}
```

- a. 3.3 b. 3.0
c. 3 d. 0.3

115. Assertion (A): There is no overflow after an addition, if one number is positive and the other is negative.

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Reason (R): Adding a positive number to a negative number always produces a result which is smaller than the larger of the two.

- a. Both A and R are true and R is the correct explanation of A
- b. Both A and R are true but R is not the correct explanation of A
- c. A is true but R is false
- d. A is false but R is true

IES-2006

116. Which block replacement algorithm is not generally used in cache operation?

- a. LIFO
- b. FIFO
- c. LRU
- d. Random

117. For which of the following devices is DMA the most suitable?

- a. Keyboard
- b. Mouse
- c. Joy stick
- d. Hard disk

118. If push and pop operation on a stack takes 1 unit time, how much time would it take to delete an element at n^{th} position from bottom?

- a. 1
- b. n
- c. n^2
- d. cannot be determined from the given

119. Self-referential structures of C programming language are very useful in applications that involve

- a. Graphs
- b. Lists
- c. Queues
- d. Stacks

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120. Which one of the following is not correct about recursion?

- a. Depth of stack is proportional to the depth of recursion
- b. Some of the recursive function cannot be written as non-recursive one
- c. For some of functions, writing recursive version is easier than non-recursive version
- d. Recursive functions have terminating conditions which limits the depth of recursion

121. Which of the following instruction of an 8086 microprocessor uses the contents of a CX register as a counter/

- a. LOCK
- b. LOOP
- c. ROTATE

select the correct answer using the code given below:

- a. Only 1 and 2
- b. Only 1 and 3
- c. Only 2 and 3
- d. 1, 2 and 3

122. Which one of the following is correct for ASCII codes of all upper case English letters compared to all lower case English letters?

- a. Are all larger
- b. Are all smaller
- c. Are all equal
- d. Some are large and some are smaller

123. Assertion (A): The development of a microprocessor based product requires the design of program and the hardware.

Reason (R): The design effort for an electronic product follows the same basic steps used in the development of software.

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- a. Both A and R are true and R is the correct explanation of A
- b. Both A and R are true but R is not the correct explanation of A
- c. A is true but R is false
- d. A is false but R is true

124. Assertion (A): Processor-level design is very much a heuristic process.

Reason (R): At this level of abstraction components are very complex

- a. Both A and R are true and R is the correct explanation of A
- b. Both A and R are true but R is not the correct explanation of A
- c. A is true but R is false
- d. A is false but R is true

125. Assertion (A): Binary search function can be easily implemented using recursion.

Reason (R): Recursion is based on number of elements in array to be searched.

- a. Both A and R are true and R is the correct explanation of A
- b. Both A and R are true but R is not the correct explanation of A
- c. A is true but R is false
- d. A is false but R is true

IES-2007

126. What does the minimizing of the memory requirement of a program mean?

- a. Maximizing number of macro calls
- b. Minimizing number of macro calls
- c. Maximizing depth of recursion
- d. Both (a) and (c) above

127. Consider the following C statements:

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```
1. x = 1; x ++ ;
2. # define max = 40;
3. x = 1; x - - ;
4. For (i = 0, i <= 1; i ++ )
{ print ( "i = % d\n");
}
```

Which of the C statements given above are not correct?

- a. 1 and 2 only b. 1, 2 and 3 only
c. 2 and 3 only d. 3 and 4 only

128. In a microcomputer, what are wait states used?

- a. To make the processor wait during a DMA operation
b. To make the processor wait during an interrupt processing
c. To make the processor wait during power shutdown
d. To interface slow peripherals to the processor

129. Which one of the following is the most suitable definition of ARRAY?

- a. it is a collection of items which share a common name
b. It is a collection of items which share a common name and occupy consecutive memory locations.
c. it is a collection of items of the same type and storage class which share a common name and occupy consecutive memory locations
d. it is just a collection of unordered items

130. Match List-I (Program Required) in System Software) with List-II

(Definition) and select the correct answer using the code given below the lists:

List-I

- a. Linker

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- b. Loader
- c. Interpreter
- d. Compiler

List-II

1. It is a program which combines smaller programs to form a single program and also links subroutines with the main program
2. It is a program which loads machine codes of a program into the system memory.
3. It is a program which translates a high level program into machine code executed it and reads one statement at a time executes and then goes to the next statements of the program
4. It is a program which translates a high level program into a machine language reads the entire program and then executes it

Codes:

	A	B	C	D
a.	1	2	3	4
b.	3	4	1	2
c.	1	4	3	2
d.	3	2	1	4

131. In which unit is the performance of cache memory measured?

- a. Hz
- b. Bits/s
- c. Cache constant
- d. Hit ratio

132. Match List-I (Type of Memory) with List-II (used as) and select the correct answer using the code given below the lists:

List-I

List-II

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- | | |
|------------------------------|------------------|
| a. DRAM | 1. Cache memory |
| b. SRAM | 2. Main memory |
| c. Parallel Access Registers | 3. BIOS memory |
| d. ROM | 4. CPU registers |

Codes:

	A	B	C	D
a.	1	2	3	4
b.	2	1	4	3
c.	1	2	4	3
d.	2	1	3	4

133. Three memory chips are of size 1 KB, 2 KB and 4 KB. Their address bus is 10 bits. What are the data bus sizes of the chips?

- a. 8 bits, 16 bits and 24 bits respectively
- b. 8 bits, 16 bits and 32 bits respectively
- c. 8 bits, 16 bits and 64 bits respectively
- d. 8 bits, 16 bits and 128 bits respectively

134. The following micro-operations are part of interrupt cycle of a control unit:

- 1. MAR \leftarrow save-address
PC \leftarrow routine address
- 2. MBR \leftarrow (PC)
- 3. Memory \leftarrow (MBR)

Which one of the following is the correct order of their occurrence?

- | | |
|----------|----------|
| a. 1-2-3 | b. 2-3-1 |
| c. 2-1-3 | d. 3-1-2 |

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135. A memory system of size 16 k bytes is required to be designed using memory chips which have 12 address lines and 4 data lines each. What is the number of such chips required to design the memory system?

- a. 2 b. 4
c. 8 d. 16

136. Assertion (A): DMA is faster than either interrupt initiated I/O or Polling based I/O for very large data transfers

Reason (R): DMA takes control of the system buses and needs no processor intervention during the data transfer.

- a. Both A and R are true and R is the correct explanation of A
b. Both A and R are true but R is not the correct explanation of A
c. A is true but R is false
d. A is false but R is true

137. Assertion (A): neumann machines are called Control Flow computers.

Reason (R): Instructions are executed sequentially as controlled by a program counter.

- a. Both A and R are true and R is the correct explanation of A
b. Both A and R are true but R is not the correct explanation of A
c. A is true but R is false
d. A is false but R is true

138. Assertion (A): Data-flow computers exploit maximum parallelism

Reason (R): Data-flow computers require no program counter

- a. Both A and R are true and R is the correct explanation of A
b. Both A and R are true but R is not the correct explanation of A

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- c. A is true but R is false
- d. A is false but R is true

139. Assertion (A): In a micro programmed CPU, each machine instruction is executed by a real time interpreter.

Reason (R): Real-time interpreter helps to achieve high degree parallelism in micro programmed control.

- a. Both A and R are true and R is the correct explanation of A
- b. Both A and R are true but R is not the correct explanation of A
- c. A is true but R is false
- d. A is false but R is true

140. For which one of the following problems recursive solution exists but non-recursive solution does not?

- a. Tower of Hanoi
- b. Factorial computation
- c. Tree traversal
- d. No such problem exists

141. Consider the following statements one binary tree:

1. A tree with n nodes has $(n-1)$ edges.
2. A labeled and rooted binary tree can be uniquely constructed given its post order and pre-order traversal results.
3. The maximum number of nodes in a binary tree of height (depth) h is $(2^{h+1} - 1)$.
4. A complete binary tree with n internal nodes has $(n+1)$ leaves.

Which of the statements given above are correct?

- a. 1, 2, 3 and 4
- b. 1, 2 and 3 only
- c. 1 and 3 only
- d. 2 and 4 only

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142. Which of the following are included in the architecture of computer?

1. Addressing modes design of CPU
2. Instructions set, data formats
3. Secondary memory, operating system

Which of the statements given above are correct?

- a. 1 and 2 only b. 2 and 3 only
c. 1 and 3 only d. 1, 2 and 3

143. Why does an increase of the RAM of a computer typically improve performance?

- a. Virtual memory increases
- b. Larger RAMs are faster
- c. Fewer page faults occur
- d. Fewer segmentation faults occur

144. Division by zero in a program gives rise to which one of the following?

- a. Syntax error b. Run-time error
c. Logical error d. Semantic error

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145. If the mantissa in the floating point representation of a number is 37 bits long then what is the accuracy of the digital computer?

- a. 37 decimal places
- b. 23 decimal places
- c. 11 decimal places
- d. 10 decimal places

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146. Which one of the following is correct? The convention is that the number 0 has normal form representation as

- a. 0 b. .0
- c. 0.0 d. 0.10^0

147. Match List-I (Pascal Operator) with List-II (C-operator) and select the correct answer using the code given below the lists:

List-I

- a. :=
- b. <>
- c. =

List-II

- 1. !=
- 2. ==
- 3. =

Codes:

	A	B	C
a.	1	2	3
b.	3	1	2
c.	2	1	3
d.	2	3	1

148. For interfacing of assembly language routines with some high level language, one must address which of the following?

- 1. How is the subroutines invoked?
- 2. How are parameters passed?
- 3. How are values returned?
- 4. How many parameters are passed?

Select the correct answer using the code given below:

- a. 1 and 3 only b. 2 and 4 only
- c. 1, 2 and 3 only d. 1, 2, 3 and 4

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149. The parallel computers are divided into which of the following architecture configurations?

1. Array processors
2. Data processors
3. Multi processor systems
4. Pipeline computers

Select the correct answer using the code given below

- | | |
|--------------------|--------------------|
| a. 1, 2 and 3 only | b. 2, 3 and 4 only |
| c. 1, 3 and 4 only | d. 1, 2 and 4 only |

150. Which one of the following is correct?

A micro program is

- a. any source program run on micro computers
- b, any set of instructions for primitive operation in a system
- c. a general name for macros used in assemble language programming
- d. any program of a very small size

151. Which are the characteristics of vertical micro instructions?

1. Considerable encoding of control information
2. Limited ability to express parallel micro operation
3. Long format

Select the correct answer using the code given below:

- | | |
|-----------------|-----------------|
| a. 1 and 2 only | b. 2 and 3 only |
| c. 1 and 3 only | d. 1, 2 and 3 |

152. A magnetic drum of 8 inch diameter has 100 tracks and storage density of 200 bits/inch. What is its storage capacity?

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- a. 8402 bits b. 202400 bits
c. 502400 bits d. 1004800 bits

153. Match List-I (Type of Memory) with List-II and select the correct answer using the code given below the lists:

List-I	List-II
a. DRAM	1. 1
b. SRAM	2. 10
c. Hard Disk	3. 100000
d. Magnetic Tape	4. 10000000

Codes:

	A	B	C	D
a.	1	2	3	4
b.	1	2	4	3
c.	2	1	3	4
d.	2	1	4	3

154. If 8085 adds 87 H and 79 H then

- a. both CARRY and zero flags will be set to 0
b. CARRY flag will be set to 0, ZERO flag to 1
c. CARRY flag will be set to 1, ZERO flag to 0
d. both CARRY and ZERO flags will be set to 1

155. On the 8085, which of the following machine cycles are not used in the CALL instruction?

1. Instruction Fetch 2. I/O
3. Memory Read 4. Memory write

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Select the correct answer using the code given below:

- a. 2 only
- b. 1 and 4
- c. 2, 3 and 4
- d. None of these

156. In 8085, if the clock frequency is 5 MHz, the time required to execute an instruction of 18 T-states is

- a. 3.0 μ s
- b. 3.6 μ s
- c. 4.0 μ s
- d. 6.0 μ s

157. Which one of the following interrupts is both level and edge sensitive?

- a. RST 7.5
- b. RST 5.5
- c. TRAP
- d. INTR

158. A group of personal computers are configured to work together for speeding up the execution of a single program in

- a. simulated evaluation
- b. cluster computing
- c. network computing
- d. client server computing

159. A memory system of size 32k bytes is required to be designed using memory chips which have 12 address lines and 4 data lines each. What is the number of such chips required to design the memory system?

- a. 4
- b. 8
- c. 16
- d. 32

160. What is an interrupt in which the external device supplies its address as well as the interrupt request known as?

- a. Vectoral interrupt

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- b. Maskable interrupt
- c. Non-maskable interrupts
- d. None of the above

161. Which one of the following is correct?

A micro program

- a. is usually written in high level language
- b. is a program for micro computers
- c. is a program written in assembly language
- d. is a sequencing program for the control unit of any processor

162. Match List-I with List-II and select the correct answer using the codes given below the lists:

List-I

- a. Immediate addressing
- b. Implied addressing
- c. Register addressing
- d. Direct addressing

List-II

- 1. LDA 30 FF
- 2. MOV A, B
- 3. LXI H, 2050
- 4. RRC

Codes:

	A	B	C	D
a.	3	4	2	1
b.	2	1	3	4
c.	3	1	2	4
d.	2	4	3	1

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1. (d)

2. (b)

3. (d)

4. (d)

5. (d)

6. (b)

7. (b)

8. (b)

Effective memory access time

$$= \text{Hit ratio} \times \text{access time in cache}$$

$$\text{Memory} + (1 - \text{Hit ratio}) \times \text{access}$$

$$\text{Time in main memory}$$

$$= 0.95 \times 10 + (1 - 0.95) \times 100$$

$$= 9.5 + 5$$

$$= 14.5 \text{ ns}$$

9. (a)

Effective memory address

$$= 1 \text{ FAB0} + 10\text{A1}$$

$$= 20\text{B51}$$

10. (d)

To have the multiprocessing capabilities, 8086 microprocessor has to operate in the maximum mode which happens when pin $\overline{MN}/\overline{MX}$ is low.

11. (b)

12. (a)

13. (b)

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14. (b)

A loader is a program which loads object code from secondary memory to main memory.

15. (c)

$x = 3954$
 $y = 0$
 $p = \text{remainder of } 3954/10$
 $p = 4$
 $x = \text{greatest integer of } 3954/10$
 $x = 395$
 $y = 0+4=4$
since $x \neq 0$, loop will continue
 $p = \text{remainder of } 395/10$
 $= 5$
 $x = \text{greatest integer of } 395/10$
 $= 39$
 $y = 4+5 = 9$
since, $x \neq 0$, loop will continue
so $p = \text{remainder of } 39/10$
 $= 9$
 $x = \text{greatest integer of } 39/10$
 $= 3$
 $y = 9+9 = 18$

since $x \neq 0$, loop will continue.

So $p = \text{remainder of } 3/10$
 $= 3$
 $x = \text{greatest integer of } 3/10$
 $= 0$

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$$y = 18 + 3 = 21$$

since $x = 0$, y has final value.

$$y = 21$$

16. (b)

17. (b)

Assembly code	Operation
LOAD X	X
MULT Y	XY
STORE T1	XY
MULT T1	$(XY)^2$
STORE T1	$(XY)^2$
LOAD Z	Z
ADD Y	Z+Y
ADD T1	$Z+Y+(XY)^2$
STORE R	$R = (XY)^2 + Y+Z$

18. (b)

19. (a)

20. (b)

21. (d)

22. (c)

23. (a)

24. (d)

Effective memory address

$$= 1FAB0 + 10 A1$$

$$= 20 B51$$

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25. (b)

26.(d)

27. (a)

28. (a)

29. (c)

30. (d)

31. (d)

32. (c)

Firmware's are the programs stored in ROMS or other devices which permanently keep their stored information.

33.(a)

34. (b)

35. (c)

36. (d)

37. (a)

38. (d)

39. (d)

All flags get affected by SUB B.

40. (c)

41. (d)

42. (d)

Most RISC instructions use register to register operations.

43. (a)

44. (b)

45. (c)

46. (d)

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The content of accumulator A will be 0 after XRA A. So zero flag will set.

47. (d)

Size of memory buffer register

$$= (24-10) = 14 \text{ bits}$$

48. (c)

49. (c)

50. (b)

51. (b)

A program that translates a high-level language program into a machine language program is called a compiler.

52. (d)

$$A = 5 + x = 10$$

$$B = 15 + y = 20$$

$$Z = 5 + 15 = 20$$

$$M = 10 \times 20 = 200$$

$$A = 5 - 15 = -10$$

$$X = 10 \times 20 = 200$$

$$B = -10 + 15 = 5$$

$$Y = -10 \times 5 = -50$$

$$Y = 200 - 50 = 150$$

$$A = 5 - (-10) = 15$$

Therefore $A = 15$, $B = 5$

53. (a)

54. (c)

55. (d)

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56. (d)

57. (b)

Register pairs are BC, DE and HL,

58. (d)

No flag changes in MOV and MVI, All flags change in ADD and CMP.

59. (b)

60. (d)

(i) IN and OUT instruction are used in I/O mapped I/O scheme.

(ii) In memory mapped I/O scheme I/O devices limit can exceed 256.

61. (c)

The most significant bit represents the sign of the number. Therefore, it is stored in the sign status flag,

62. (d)

63. (a)

64.(a)

65. (a)

66.(d)

67.(c)

68. (c)

69. (c)

70.(c)

71. (a)

72. (c)

73.(b)

74. (b)

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75. (c)

PUSH a = Put a on the stack

PUSH B = Put b on the stack

PUSH c = Put c on the stack

POP AX = Store c in AX

POP BX = Store b in BX

SUB AX, BX= Store c-b in AX

POP BX = Store a in BX

ADD AX, BX = Store c-b +a in AX

76. (d)

77. (d)

78. (a)

79. (a)

80. (a)

81. (b)

82. (c)

83.(a)

84. (d)

85.(d)

86.()

87. (a)

88. (d)

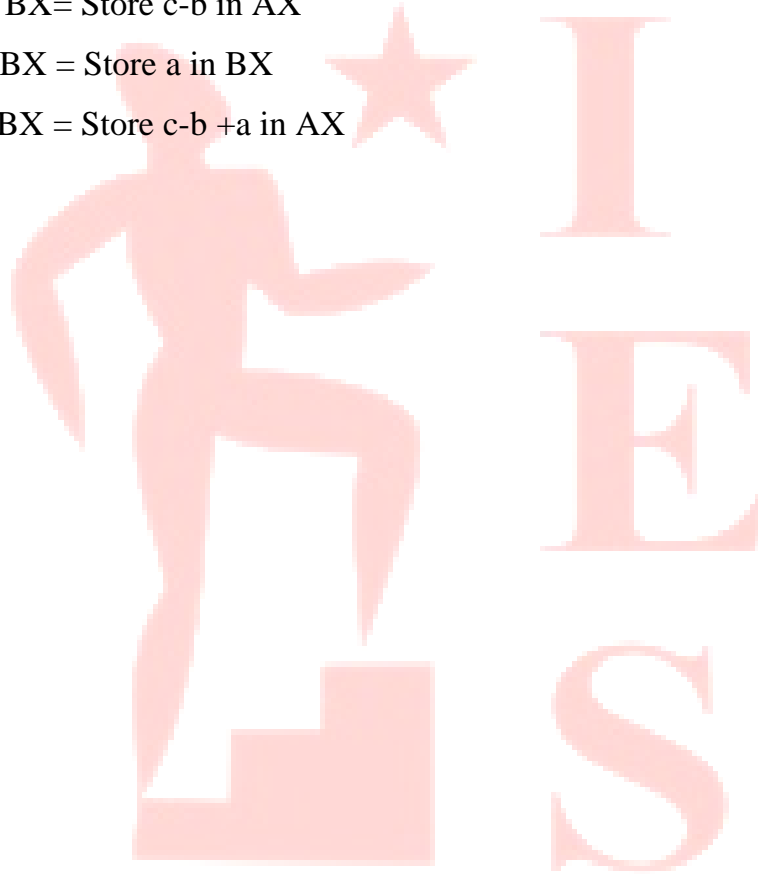
89. ()

90.(a)

91. ()

92. ()

93. (b)



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94.(d)

95. ()

96.(c)

97.(d)

98.(b)

99. (a)

100. (a)

101. (a)

102. (b)

103. (c)

104.(b)

105. (b)

106. (d)

107. (d)

108. (b)

Machine cycles of PUSH B instruction are shown below

<i>Fetch</i>	<i>Write</i>	<i>Write</i>
$6 - Tstates$	$3 - T$	$3 - T$

109. (a)

110. (b)

111. (a)

112. (a)

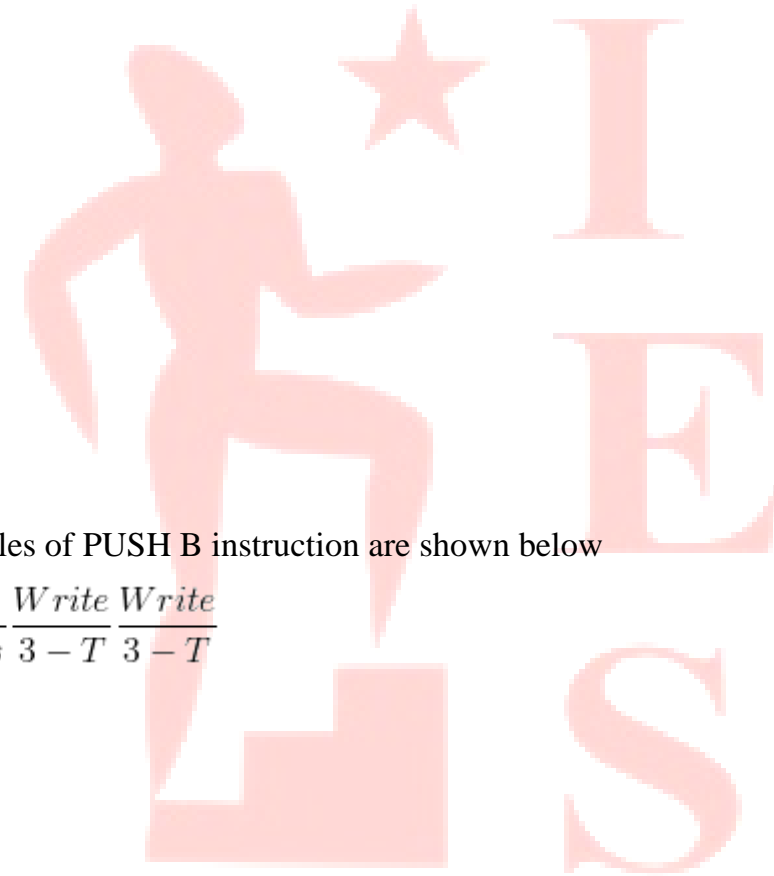
113. (a)

114. (a)

115. (a)

116. (b)

117. (d)



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118. (d)

119. (a)

120. (b)

121. (c)

122. (b)

123. (b)

124. (d)

125. (c)

126. (b)

127. (c)

128. (d)

129. (c)

130. (a)

131. (d)

132. (b)

133. (b)

Data bus size = $\frac{\text{Memory chip size}}{\text{Address bus size}}$

For 1 KB memory chips

$$\text{data bus size} = \frac{2^{10} \times 8}{2^{10}} = 8\text{bits}$$

For 2 KB memory chip

$$\text{data bus size} = \frac{2 \times 2^{10} \times 8}{2^{10}} = 16\text{bits}$$

For 4 KB memory chip

$$\text{data bus size} = \frac{4 \times 2^{10} \times 8}{2^{10}} = 32\text{bits}$$

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134. (d)

135. (c)

Number of chips required

$$= \frac{16 \times 2^{10} \times 8}{2^{12} \times 4} = 8$$

136.(a)

137. (a)

138. (c)

139. (c)

140. (d)

141. (c)

142. (a)

143. (c)

144. (b)

145. (c)

146. (c)

147. (b)

148. (c)

149. (c)

150. (b)

151. ()

152. (c)



Storage capacity

$$= \pi \times \text{diameter} \times \text{tracks} \times \text{storage density}$$

$$= 3.14 \times 8 \times 100 \times 200$$

$$= 502400 \text{ bits}$$

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153. (c)

154. (d)

$$87 \text{ H} = 10000111$$

$$79 \text{ H} = 01111001$$

$$\begin{array}{r} 1000\ 0111 \\ +0111\ 1001 \\ \hline 1\ 00000000 \\ \hline \end{array}$$

Carry 8-bit sum

Therefore both Carry and zero flags will be set to 1.

155. (a)

Machine cycles of Call instruction are given below

<i>Fetch</i>	<i>Read</i>	<i>Read</i>	<i>Write</i>	<i>Write</i>
$6T - \text{states}$	$3T$	$3T$	$3T$	$3T$

156. (b)

Clock frequency $f = 5 \text{ MHz}$

Time required to execute 1 T- state

$$t = \frac{1}{f}$$

Time required to execute 18 T-states.

$$\begin{aligned} T &= 18t \\ &= \frac{18}{f} = \frac{18}{5 \times 10^6} = 3.6 \mu\text{s} \end{aligned}$$

157. (c)

TRAP is level triggered as well as edge triggered interrupt.

158. (b)

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159. (c)

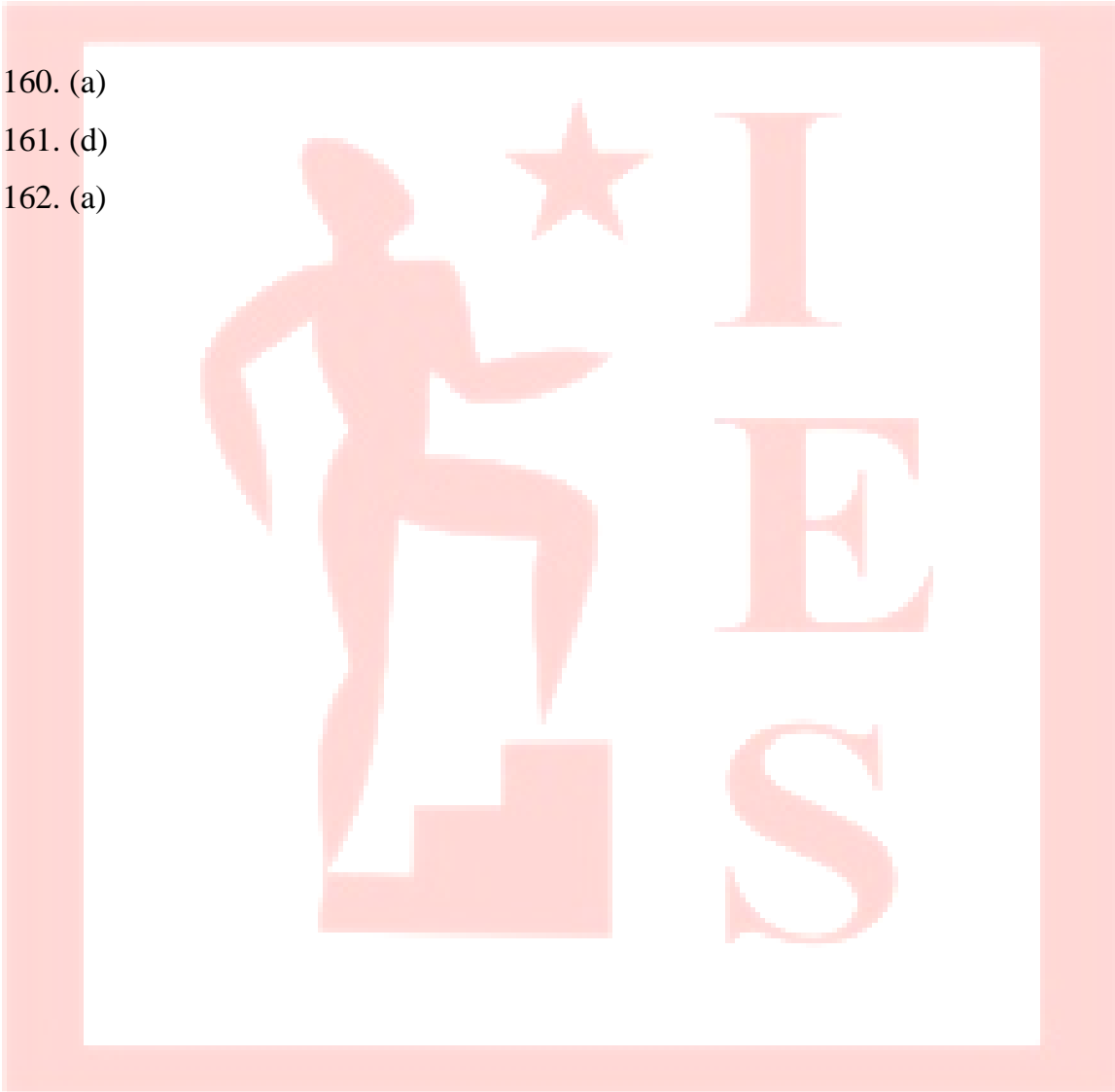
Number of chips required

$$= \frac{32 \times 1024 \times 8}{2^{12} \times 4} = 16$$

160. (a)

161. (d)

162. (a)



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