

1. The number of hardware interrupts (which require an external signal to interrupt) present in an 8085 microprocessor are
 (a) 1 (b) 4 (c) 5 (d) 13
2. In the 8085 microprocessor, the RST6 instruction transfers the program execution to the following location:
 (a) 30H (b) 24H (c) 48H (d) 60H
3. The contents of Register (B) and Accumulator (A) of 8085 microprocessor are 49H and 3AH respectively. The contents of A and the status of carry flag (cy) and sign flag (S) after executing SUB B instructions are
 (a) A = F1, CY=1, S= 1 (b) A = 0F, CY= 1, S= 1, (C) A= F0, CY= 0, S=0 (d) A=1F, CY =1, S= 1
4. Consider the following assembly language program.
 MV B, 87H
 MOV A, B
 START: JMP NEXT
 MVI B, 00H
 XRA B
 OUT PORT 1
 HLT
 NEXT: XRA B
 JP START
 OUT PORT 2
 HLT
- The execution of the above program in an 8085 microprocessor will result in
 (a) an output of 87H at PORT1 (b) an output of 87H at PORT 2
 (c) infinite looping of the program execution with accumulator data remaining at 00H
 (d) infinite looping of the program execution with accumulator data alternating between 00H and 87H
5. In an 8085 microprocessor, the instruction CMP B has been executed. While the content of the accumulator is less than that of register B. As a result
 (a) Carry flag will be set but Zero flag will be reset (b) Carry flag will be reset but Zero flag will be set
 (c) Both Carry flag and Zero flag will be reset (d) Both Carry flag and Zero flag will be set
6. The 8255 Programmable Peripheral interface is used as described below.
 (I) An A/D converter is interfaced to a microprocessor through an 8285. The conversion is initiated by a signal from the 8255 on port C. A signal on Port C causes data to be strobed into Port A
 (II) Two computers exchange data using a pair of 8255s. Port A works as a bidirectional data port supported by appropriate handshaking signals
 The appropriate modes of operation of the 8255 for (I) and (II) would be
 (a) Mode 0 for (I) and Mode 1 for (II) (b) Mode 1 for (I) and Mode 0 for (II)
 (c) Mode 2 for (I) and Mode 0 for (II) (d) Mode 2 for (I) and Mode 1 for (II)
7. The number of memory cycles required to execute the following 8085 instruction
 (I) LDA 3000 H
 (II) LXI D, F0F1 H
 Would be
 (a) 2 for (I) and 2 for (II) (b) 4 for (I) and 3 for (II) (c) 3 for (I) and 3 for (II) (d) 3 for (I) and 4 for (II)
8. Consider the sequence of 8085 instructions given below.
 LXI H, 9258, MOV A, M, CMA, MOV M, A
 Which one of the following is performed by this sequence?
 (a) Contents of location 9258 are moved to the accumulator
 (b) Contents of location 9258 are compared with the contents of the accumulator
 (c) Contents of location 9258 are complemented and stored in location 9258
 (d) Contents of location 5892 are complemented and stored in location 5892
9. It is desired to multiply the numbers 0AH by 0BH and store the result in the accumulator. The numbers are available in registers B and C respectively. A part of the 8085 program for this purpose is given below:
 MVI A, 00H
 Loop:

.....

 HLT END

The sequence of instruction to complete the program would be

- (a) JNZ LOOP ADDB, DCR C
 (b) ADD B, JNZ LOOP DCR C
 (c) DCR C, JNZ LOOP ADD B
 (d) ADD B, DCR C JNZ LOOP

Common data for Questions 10 and 11

Consider an 8085 microprocessor system

10. The following program starts at location 0100H.

LXI SP, 00FF
 LXI H, 0107
 MVI A, 20H
 SUB M

The content of accumulator when the program counter reaches 0109H is

- (a) 20 H (b) 02 H (c) 00H (d) FFH

11. If in addition following code exists from 0109H onwards,

ORI 40 H
 ADD M

What will be the result in the accumulator after the last instruction is executed?

- (a) 40H (b) 20 H (c) 60 H (d) 42 H

12. Following is the segment of a 8085 assembly language program:

LXI SP, EFFFH
 CALL 3000H
 3000H: LXIH, 3CF4H
 PUSH PSW
 SPHL
 POP PSW
 RET

On completion of RET execution, the contents of SP is

- (a) 3CFOH (b) 3CF8H (c) EFFDH (d) EFFFH

Statement for linked answer Questions 13 & 14 :

An 8085 assembly language program is given below.

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Line 1: MVI A, B5H
 2: MVI B, 0EH
 3: XRI 69H
 4: ADD B
 5: ANI 9BH
 6: CPI 9FH
 7: STA 3010H
 8: HLT

13. The contents of the accumulator just after execution of the ADD instruction in line 4 will be

- (a) C3H (b) EAH (c) DCH (d) 69H

14. After execution of line 7 of the program, the status of the CY and Z flags will be

- (a) CY= 0, Z= 0 (b) CY= 0, Z= 1 (c) CY= 1, Z= 0 (d) CY= 1, Z= 1

15. An 8085 executes the following instructions

2710 LXI H, 30A0H
 2713 DAD H
 2714 PCHL

All addresses and constants are in Hex. Let PC be the contents of the program counter and HL be the contents of the HL registers pair just after executing PCHL.

Which of the following statements is correct?

- (a) PC = 2715H HL =60A0H (b) PC = 30A0H HL =2715H
 (c) PC =6140H HL =6140H (d) PC =6140H HL =2715H

16. In a microprocessor, the service routine for a certain interrupt starts from a fixed location of memory

Which cannot be externally set, but the interrupt can be delayed or rejected. Such an interrupt is

- (a) non-maskable and non- vectored (b) maskable and non- vectored
 (c) non-maskable and vectored (d) maskable and vectored

17. Which one of the following instructions is a 3-byte instruction ?

- a) MVI A b) LDA X B c) JMP 2050 d) MOV A,M

18. How many times will the following loop be executed ?

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                LXI B          0010 H
LOOP:          DCX           B
                MOV           A,B
                ORA           C
                JNZ           LOOP
  
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Select the correct answer using the code given below :

- a) 10 b) 100 c) 16 d) 15

19. The power failure alarm must be connected to which one of the following interrupt of 8085 ?

- a) RST 7.5 b) TRAP c) INTR d) HOLD

20. What are the sets of commands in a program which are not translated into machine instructions during assembly process, called ?

- a) Mnemonics b) Directives c) Identifiers d) Operands

21. Both the ALU and control section of CPU employ which special purpose storage locations ?

- a) Buffers b) Decoders c) Accumulators d) Registers

22. In an Intel 8085 A, which is always the first machine cycle of an instruction ?

- a) An op-code fetch cycle b) A memory read cycle c) A memory write cycle d) An I/O read cycle

23. The addressing mode used in the instruction JMP F 347 H in case of an Intel 8055 A microprocessor in which one of the following ?

- a) Direct b) Register – indirect c) Implicit d) Immediate

24. What is the number of machine cycles in the instruction LDA 2000 H that consists of thirteen states ?

- a) 2 b) 3 c) 4 d) 5

25. An Intel 8085 A microprocessor is operated at a frequency of 2 MHz . If the instruction LXI H, E000 H that takes ten 'T' states , is executed , then what is the instruction cycle time ?

- a) 10 μ s b) 5 μ s c) 4 μ s d) 2.5 μ s

26. When TRAP interrupt is triggered in an Intel 8085 A, the program control is transferred to which one of the following ?

- a) 0020 H b) 0024 H c) 0028 H d) 002C H

27. The contents of program Counter (PC), when the microprocessor is reading from 2FFF H memory location , will be

- a) 2FFE H b) 2FFF H c) 3000 H d) 3001 H

28. Carry flag is not affected after the execution of

- a) ADD B b) SBB B c) INR B d) ORA B

29. Which one is the indirect addressing mode in the following instructions ?

- a) LXIH 2050 H b) MOV A,B c) LDAX B d) LDA 2050 H

30. An 8254 programmable interval timer consists of independent 16-bit programmable counters . This number is

- a) 2 b) 3 c) 4 d) 5

Answers:

- | | |
|-----|----------|
| 1. | <u>C</u> |
| 2. | <u>A</u> |
| 3. | <u>A</u> |
| 4. | <u>B</u> |
| 5. | <u>A</u> |
| 6. | <u>D</u> |
| 7. | <u>B</u> |
| 8. | <u>C</u> |
| 9. | <u>D</u> |
| 10. | <u>C</u> |
| 11. | <u>C</u> |
| 12. | <u>B</u> |
| 13. | <u>B</u> |
| 14. | <u>C</u> |
| 15. | <u>C</u> |
| 16. | <u>D</u> |
| 17. | <u>C</u> |
| 18. | <u>C</u> |
| 19. | <u>B</u> |
| 20. | <u>B</u> |
| 21. | <u>C</u> |
| 22. | <u>A</u> |
| 23. | <u>D</u> |
| 24. | <u>C</u> |
| 25. | <u>B</u> |
| 26. | <u>B</u> |
| 27. | <u>C</u> |
| 28. | <u>C</u> |
| 29. | <u>C</u> |
| 30. | <u>B</u> |