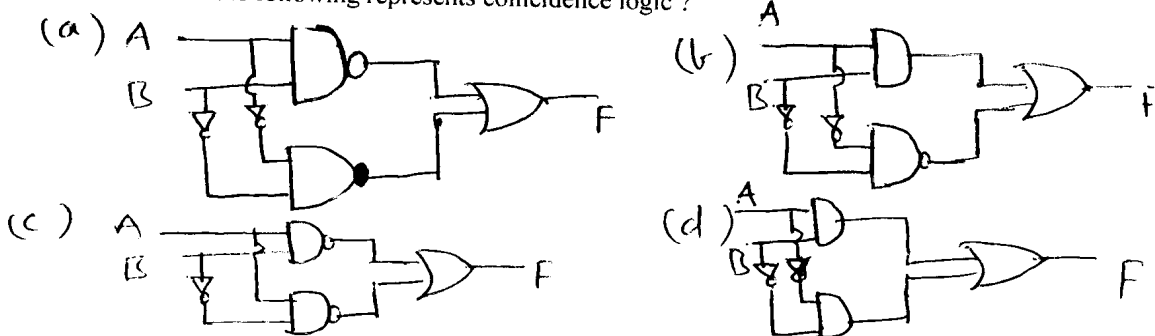


1. The Boolean expression $A.B + \bar{A}.\bar{B}$ is logically equivalent to
 A. $(A + \bar{B}) . (\bar{A} + B)$ B. $(\bar{A} + \bar{B}) . (A + B)$ C. $A.\bar{B} + \bar{A}.B$ D. $\bar{A}.\bar{B} + \bar{A}.\bar{B}$
 of these, correct expression is
 a. all b. A,B c. C,D d. A,C

2. Which one of the following represents coincidence logic ?

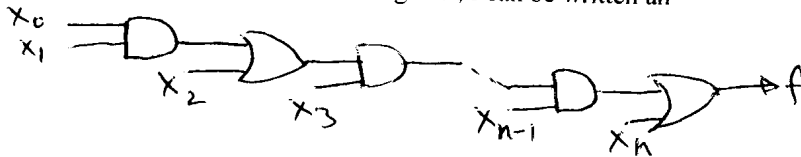


3. The simplified Boolean expression associated with the K-map shown in figure (X indicate 'don't care') is

		A/B			
	C/D	00	01	11	10
00		0	0	1	1
01		0	X	X	1
11		X	X	1	X
10		1	0	1	1

- a. $\bar{A} + \bar{B}C$ b. $A + \bar{B}C$ c. $ABC + A\bar{D}$ d. $A + \bar{A}BCD$

4. In the given network of AND and OR gates, f can be written as



- a. $x_0x_1x_2 \dots x_n + x_1x_2 \dots x_n + x_2x_3 \dots x_n + \dots + x_n$ b. $x_0x_1 + x_2x_3 + \dots + x_{n-1} \dots x_n$
 $x_1 + x_2 + \dots + x_n$ d. $x_0x_1x_3 \dots x_{n-1} + x_2x_3x_5 \dots x_{n-1} + \dots + x_{n-2}x_{n-1} + x_n$ c. $x_0 +$

5. For the circuit shown below, output

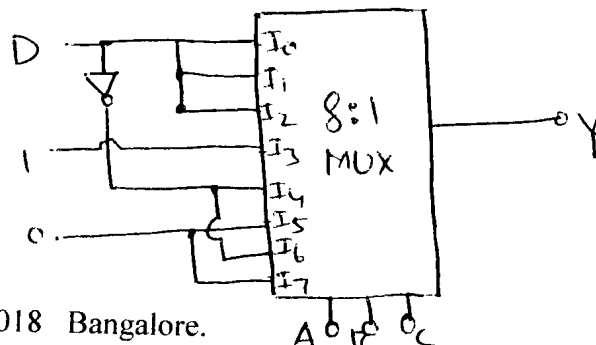


- a) $F = 1$ b. $F = 0$ c. $F = X$ d. $F = \bar{X}$

6. The digital multiplexer is basically a combinational logic circuit to perform the operation

- a. AND-AND b. OR-OR c. AND-OR d. OR-AND

7. For the given multiplexer, Y is equal to

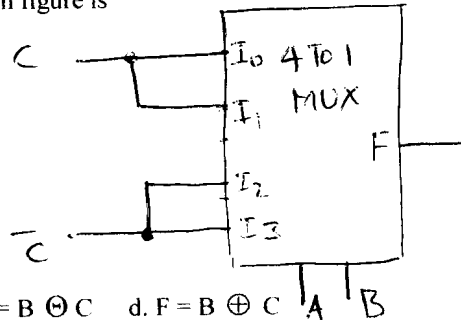


a. $\overline{A}\overline{C}\overline{D} + \overline{A}BC + \overline{A}D$
 d. $\overline{A}\overline{C}\overline{D} + \overline{A}BD + \overline{A}D$

b. $\overline{A}BC + \overline{A}\overline{C}\overline{D} + \overline{A}D$

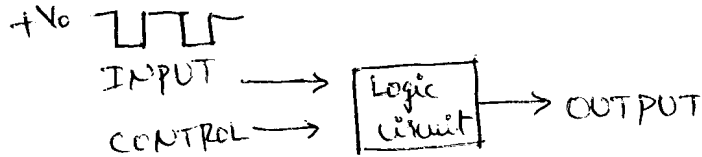
c. $\overline{A}BC + \overline{A}\overline{C}\overline{D} + \overline{A}D$

8. The logic realized by the circuit shown in figure is



- a. $F = A \oplus C$ b. $F = A \oplus C$ c. $F = B \oplus C$ d. $F = B \oplus C$

9. In the combinational logic circuit shown in the given figure, the input square wave is phase-inverted at the output when the control input is 1. It is passed on as it is when the control input is 0. It is passed on as it is when the control input is 0. The logic circuit is a 2-input



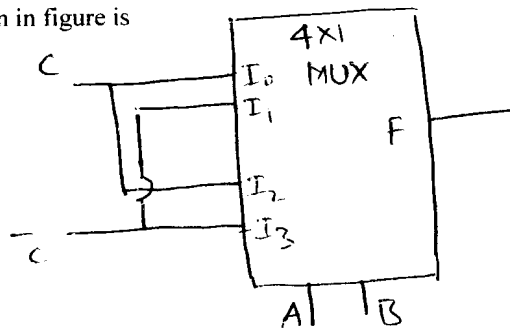
- A. NAND gate b. NOR gate c. Exclusive OR gate d. Exclusive NOR gate

10. If the input to the digital circuit (in the figure) consisting of a cascade of 20 XOR-gates is X, then the output Y is equal to



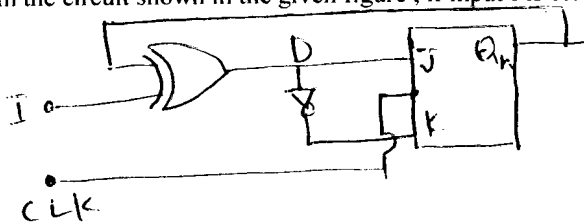
- a. 0 b. 1 c. \overline{X} d. X

11. The logic realized by the circuit shown in figure is



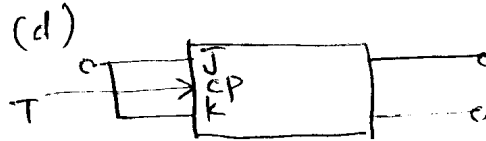
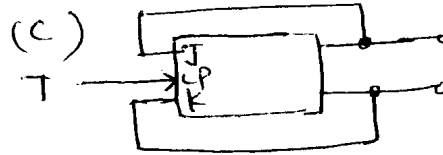
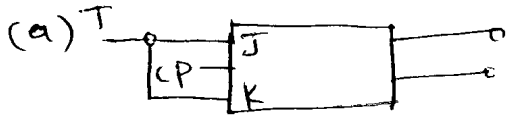
- a. $F = A \cdot C$ b. $F = A \oplus C$ c. $F = B \cdot C$ d. $F = B \oplus C$

12. In the circuit shown in the given figure, if input I is set high, output Q_{n+1} becomes



- a. \overline{Q}_n b. Q_n c. high d. low

13. Which one of the circuits given below converts a JK FF to a T FF ?



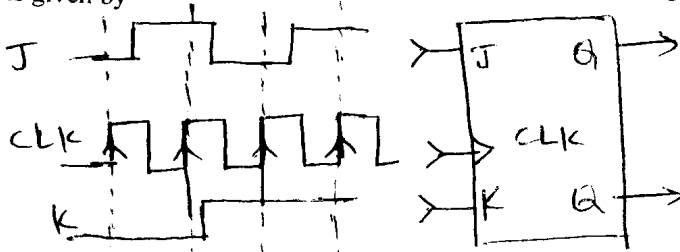
14. In FF clocking

- a. Hold time is greater than set up time
- b. Set up time is greater than hold time
- c. Hold time is before edge triggering
- d. Set up time is after edge triggering

15. The output of a Moore sequential machine is a function of

- a. All present states of the machine
- b. All the inputs
- c. A few combination of inputs and the present state
- d. All the combinations of inputs and the present state

16. The J-K flip-flop shown in figure is initially reset, so that $Q = 0$. If a sequence of four clock pulses is then applied, with the J and K inputs as given in the figure, the resulting sequence of values that the output Q will have is given by



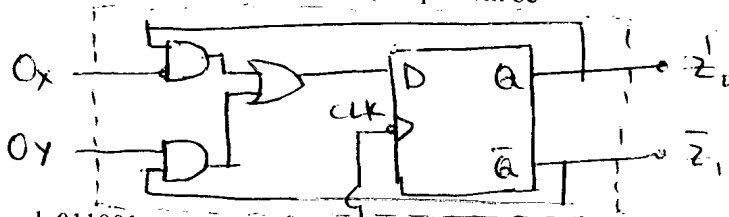
- a. 01011
- b. 01010
- c. 00110
- d. 00101

17. The characteristic equation for the next state (Q_{n+1}) of a J-K flip-flop is

- a. $Q_{n+1} = JQ_n + K\bar{Q}_n$
- b. $Q_{n+1} = JQ_n + KQ_n$
- c. $Q_{n+1} = J\bar{Q}_n + KQ_n$
- d. $Q_{n+1} = JQ_n + KQ_n$

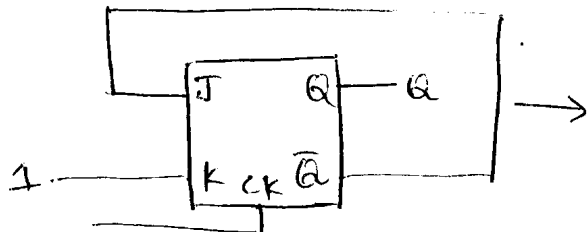
(where Q_n represents the present state)

18. In a J-K flip-flop we have $J = \bar{Q}$ and $K = 1$ (see fig). Assuming the flip flop was initially cleared and then clocked for 6 pulses, the sequence at the Q output will be



- a. 010000
- b. 011001
- c. 010010
- d. 010101

19. A sequential circuit using D flip-flop and logic gates is shown in fig. Where X and Y are the inputs and Z is the output. The circuit is



- a. S-R Flip-Flop with inputs $X = R$ and $Y = S$
- b. S-R Flip-Flop with inputs $X = S$ and $Y = R$
- c. J-K Flip-Flop with inputs $X = J$ and $Y = K$
- d. J-K Flip-Flop with inputs $X = K$ and $Y = J$

20. If

$t_p \rightarrow$ duration of the clock pulse

$\Delta t \rightarrow$ propagation delay
 $T \rightarrow$ clock period

Then to avoid race-around condition occurring with J-K flip-flop

- a. $t_p = \Delta t = T$ b. $t_p > \Delta t = T$ c. $t_p < \Delta t < T$ d. $t_p < \Delta t = T$

21. A pulse train can be delayed by a finite number of clock periods using

- a. a serial-in , serial – out shift register b. a serial-in , parallel – out shift register
 c. a parallel-in , serial – out shift register d. a parallel-in , parallel – out shift register

22. A 4- bit modulo-16 ripple counter uses JK flip-flops. If the propagation delay of each FF is 50 ns, the maximum clock frequency that can be used is equal to

- a. 20 MHz b. 10 MHz c. 5 MHz d. 4 MHz

23. A divide –by-78 counter can be realized by using

- a. 6 nos of mod-13 counters b. 13 nos of mod-6 counters c. one mod-13 counter followed by one mod-6 counters d. 13 nos of mod-13 counters

24. The number of unused states in a 4-bit Johnson counter is

- a. 2 b. 4 c. 8 d. 12

25. A pulse train with a frequency of 1 MHz is counted using a modulo 1024 ripple-counter built with J-K flip-flops. For proper operation of the counter. The maximum permissible propagation delay per flip-flop stage is..... n sec.

- a. 100 b. 50 c. 20 d. 10

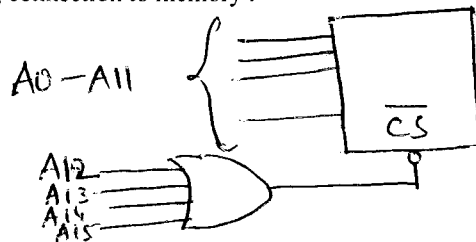
26. For each of the following statements, indicate the type (s) of counter being described.

- A. The total switching delay is the sum of the individual FFs delays 1. Asynchronous counter
 B. This counter requires no decoding Logic 2. Ring counter
 C. This counter can begin its counting Sequence at any desired starting state 3. presetable counter
 D. This counter can be designed to count through arbitrary sequences by determining logic needed at each flip-flop’s J and K input 4. synchronous counter

Codes :

	A	B	C	D
(a)	1	2	3	4
(b)	4	2	3	1
(c)	1	3	2	1
(d)	4	3	2	1

27. Consider the following connection to memory :



The accessible range of address from the memory is

- a. 0000-0FFF b. 1FFF-4FFF c. 0000-FFFF d. 0000-4FFF

28. Match List-I (computer terms) with List-II(definitions) and select the correct answer using the codes given below the lists :

List- I

- A. Semiconductor memory
 B. Ferrite core memory
 C. Magnetic type memory
 D. Read-only memory

List-II

1. Destructive read out
 2. Combinational
 3. Volatile
 4. Non-volatile

Codes :

	A	B	C	D
(a)	3	1	4	2
(b)	2	3	1	4
(c)	4	3	1	2
(d)	2	4	3	1

29. Four memory chips of 16 x 4 size have their address buses connected together. The resulting memory system will be of size

- a. 64 x 4 b. 16 x 16 c. 32 x 8 d. 256 x 1

30. How many steps are there in the output of a 10-bit D/A converter ?

- a. 1023 b. 1024 c. 10 d. 100

31. The resolution of an 8-bit optical encoder is

- a. 0.7° b. 1.4° c. 2.8° d. 3.6°

32. The resolution of a 4-bit counting ADC is 0.5 volts. For an analog input of 6.6 volts, the digital output of the ADC will be

- a. 1011 b. 1101 c. 1100 d. 1110

33. The number of comparators in a 4 bit flash ADC is

- a. 4 b. 5 c. 15 d. 16

34. In a 4-bit weighted-resistor A/D converter, the resistor value corresponding to LSB is 32 K Ω . The resistor value corresponding to MSB will be

- a. 32 K Ω b. 16 K Ω c. 8 K Ω d. 4 K Ω

35. Match List -I (types of A/D converters) with List-II (properties of A/D converters) and select the correct answer using the codes given below the lists :

List - I

List -II

- | | |
|-----------------------------|--|
| A. Dual slope | 1. Fixed conversion time; depends on the no. of bits |
| B. Counter-Ramp | 2. High speed operation |
| C. Successive approximation | 3. Hum rejection |
| D. Simultaneous | 4. Conversion time dependent on signal amplitude |
| | 5. Large conversion time |

Codes :

	A	B	C	D
(a)	3	2	5	4
(b)	2	3	4	1
(c)	3	4	1	2
(d)	4	1	2	5

36. A D/A converter has 5 V full-scale output voltage and an accuracy of $\pm 0.2\%$. The maximum error for any output voltage (accuracy = $LSB / 2$)

- a. will be 2 mV b. will be 10 mV c. will be 20 mV d. can be of any value depending on input

37. If the input to a 5 bit ladder type DAC is 11101 (where '0' and '1' represents 0V and 10 V respectively), the output voltage will be approximately

- a. 1 V b. +9 V c. -9 V d. +10 V

38. Among the logic families, the family which can be used at very high frequency greater than 100 MHz in a 4 bit synchronous counter is

- a. TTLAS b. CMOS c. ECL d. TTL

39. The gate delay of an NMOS inverter is dominated by charge time rather than discharge time because

- a. The driver transistor has larger threshold voltage than the load transistor
 b. the driver transistor has large leakage currents compared to the load transistor
 c. the load transistor has a small W/L ratio compared to the driver transistor
 d. none of these

40. The noise margin of a TTL gate is about

- a. 0.2 V b. 0.4 V c. 0.6 V d. 0.8 V

41. Match List -I (computer terms) with List -II(definitions) and select the correct answer using the codes given below the lists

List - I

List- II

- | | |
|---------|---|
| A. TTL | 1. Non saturation type and high power consumption |
| B. ECL | 2. Low power consumption and high packing density |
| C. CMOS | 3. High switching speed and good fan-out capability |

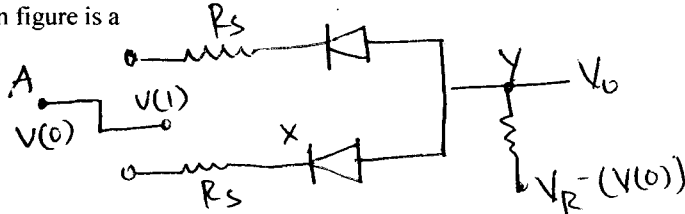
D. I²L

4. Bipolar logic with high packing density

Codes:

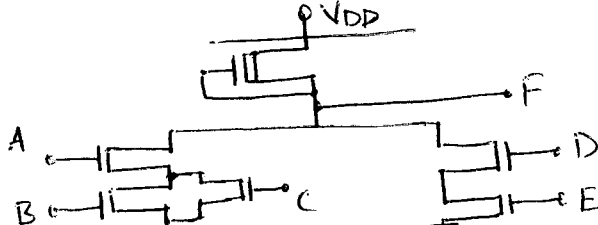
	A	B	C	D
(a)	3	1	2	4
(b)	2	3	1	4
(c)	4	3	1	2
(d)	4	3	2	1

42. The circuit shown in the given figure is a



- a. positive logic OR circuit b. negative logic OR circuit c. positive logic NAND circuit
 d. negative logic NAND circuit

43. For the NMOS logic gate shown in figure, the logic function implemented is

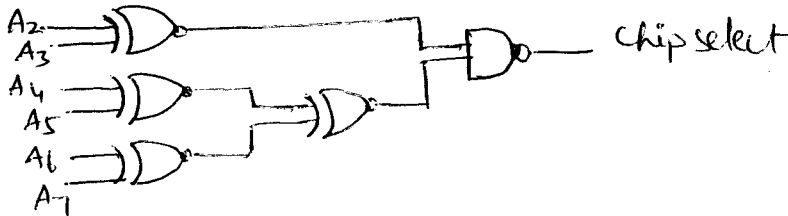


- a. ABCDE b. $(\overline{A}B + C)(D + E)$ c. $A.(B + C) + D.E$ d. $(A + B).C + \overline{D}.E$

44. Hamming codes are used for error detection and correction. If the minimum Hamming distance is m, then the number of errors correctable is

- a. equal to m b. less than m/2 c. equal to 2m d. greater than m

45. The decoding circuit shown in fig has been used to generate the active low chip select signal for a microprocessor peripheral. (The address lines are designated A₀ to A₇ for I-O addresses)



The peripheral will correspond to IO addresses in the range

- a. 60 H to 63 H b. A4 H to A7H c. 30 H to 33 H d. 70 H to 73 H

DIGITAL TEST:

1.d	2.d	3.b	4.d	5.b	6.c	7.a	8.b	9.c	10.b	11.d	12.a	13.a
	14.b	15.a	16.d	17.c	18.d	19.d	20.c	21.a	22.c	23.c	24.c	25.a
	26.a	27.a	28.a	29.b	30.a	31.b	32.d	33.c	34.d	35.c	36.b	37.b
	38.c	39.c	40.b	41.d	42.b	43.c	44.b	45.a				